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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/560,408

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Kauko O. Laakkonen

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EXAMINER

CRAWFORD, JACINTA M

ART UNIT

PAPER NUMBER

2628

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/560,408	Applicant(s) LAAKKONEN, KAUKO O.	
	Examiner JACINTA CRAWFORD	Art Unit 2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 March 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4, 6-9 and 11-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-9 and 11-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 13, 2009 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 4, 6-9, 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Valentaten et al. (US 5,250,940) in view of Ikeda (US 6,734,863).

As to claim 1, Valentaten et al. disclose an apparatus for connection between a display device and a processor controlling the display device, comprising: a memory bus for connection to the processor (Figure 2 notes the bus (RAM bus) to processor, 14), and an adaptor circuit (Figure 2, RAM arbiter, 18) for connection between the memory bus (RAM bus) and a display device connection interface (Figure 2, video circuit, 16), wherein the memory bus provides the adaptor circuit a plurality of control signal lines for writing or reading data to or from the display device, and a plurality of data signal lines carrying the data (column 3, lines 51 thru column 4, lines 22 notes various signals generated and provided throughout the system, including signals to read and write to and from RAM memory) wherein the adaptor circuit provides the display device connection interface a read signal line, a write signal line, an address signal line indicating where on the display device the data should be read or written, and a plurality of data signal lines carrying the data (column 3, lines 51 thru column 4, lines 22 notes various signals generated and provided throughout the system, including signals to read and write to and from RAM memory, where the adapter circuit (RAM arbiter) provides the display device connection interface (video circuit) access to RAM memory).

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Valentaten et al. differs from the invention defined in claim 1 in that Valentaten et al. do not expressly disclose said display device connection interface being integrated in the display device, and wherein the adaptor circuit is configured to convert an update instruction from the processor into an instruction to the display device in a timing order required by the display device for updating only a required part of the display device.

Ikeda discloses said display device connection interface being integrated in the display device (Figure 5, driving control circuit, 28 of display apparatus, 3, which is a detailed description of display apparatus of Figure 1), and wherein the adaptor circuit is configured to convert an update instruction from the processor into an instruction to the display device in a timing order required by the display device for updating only a required part of the display device (Figure 1, display controller, 2 is considered an “adapter circuit,” column 5, lines 23-40 notes converting instructions from host CPU 1 (processor) for display apparatus 3; the refresh control circuit, 10, to control timing and updating). Ikeda also discloses wherein the adaptor circuit provides the display device connection interface a read signal line, a write signal line, an address signal line indicating where on the display device the data should be read or written, and a plurality of data signal lines carrying the data (column 6, lines 48-67).

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It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Valentaten et al.'s adapter circuit with Ikeda's method of converting update instructions to appropriately and accurately output data on a display device.

As to claim 4, Valentaten modified with Ikeda disclose the apparatus wherein the memory bus is configured to realize signaling between the processor and a memory unit, as well as between the processor and the display device connection interface (Valentaten, column 3, lines 56-64 and column 4, lines 23-37).

As to claim 6, Valentaten modified with Ikeda do not expressly disclose the apparatus wherein the adapter circuit comprises one or more gates, said gates are configured to match respective signals between the memory bus and the display device connection interface.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate logic gates as logic gates are an integral part of digital circuitry.

As to claim 7, Valentaten modified with Ikeda disclose the apparatus comprising an interference protection block connected between the adapter

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circuit and the display device connection interface, said interference protection block being configured to prevent electric interferences among signals (The instant specification describes this as known).

Claims 8 and 12 are similar in scope to claim 1, and are therefore rejected under similar rationale.

Claim 9 is similar in scope to claim 4, and is therefore rejected under similar rationale.

As to claim 11, Valentaten modified with Ikeda disclose the memory bus and the display device connection interface to be connected by glue logics together in order to achieve communication there between (Valentaten, Figure 2).

Claims 13 and 14 are similar in scope to claim 6, and is therefore rejected under similar rationale.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Valentaten et al. (US 5,250,940) in view of Ikeda (US 6,734,863) as applied to claim 1 above, and further in view of Leung (US 6,760,444).

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Claim 2 requires the display device connection interface to be a medium speed screen interface.

While Valentaten et al. is used to a display device connection, it is noted that Valentaten does not express a medium speed screen interface. However, Leung teaches the use of low medium and high speed interfaces at column 9, lines 36-39, 56-67 and column 10, lines 8-10. It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the system to have a medium speed screen interface to facilitate proper establish communication among the devices.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Valentaten et al. (US 5,250,940) in view of Ikeda (US 6,734,863) as applied to claim 1 above, and further in view of Niimura et al. (US 7,116,304).

Claim 3 further requires the memory bus connected to the processor to be a non-synchronized memory bus. While Valentaten et al. is used to teach the memory bus connected to the processor, it is noted that Valentaten does not express a non-synchronized memory bus. Niimura et al. teach this at the abstract. It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the system to have a non-synchronized

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memory bus to provide a bus that is not bandwidth restricted and to reduce the overall power consumption of the system.

Response to Arguments

6. Applicant's arguments with respect to independent claims 1, 8, and 12 have been considered but are moot in view of the new ground(s) of rejection. Applicants argue on pages 6-9 of the amendment filed March 13, 2009 that the prior art cited does not teach all of the limitations of the independent claims, more specifically, "wherein the adaptor circuit is configured to convert an update instruction from the processor into an instruction to the display device in a timing order required by the display device for updating only a required part of the display device." However, Ikeda is used to teach this newly amended limitation, and is used in combination with Valentaten et al. to teach all of the limitations of the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JACINTA CRAWFORD whose telephone number is (571)270-1539. The examiner can normally be reached on M-F 8:00a.m. - 5:00p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jacinta Crawford/
Examiner, Art Unit 2628

/Kee M Tung/
Supervisory Patent Examiner,
Art Unit 2628